2018 IEEE Asia Pacific Conference on Circuits and Systems

2018 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics

Conference Program

Organized by
IEEE  CAS

Sponsored by
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Welcome Remarks

Welcome to IEEE APCCAS 2018 & PrimeAsia 2018!

On behalf of the Organizing Committee, it is my pleasure to welcome all our symposium delegates and distinguished speakers to the 14th IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2018) and 2018 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia) at the Shangri-La Hotel, Chengdu, China from Oct 26-30, 2018. Chengdu is the capital of China’s southwest Sichuan Province, the home of cute giant pandas. Benefiting from Dujiangyan Irrigation Project which was constructed in 256 B.C., Sichuan Province is reputed as the Heavenly State, a place richly endowed with natural resources.

It is a major international forum established by the IEEE Circuits and Systems Society for researchers to exchange their latest findings in circuits and systems. They bring together a diverse community to share ideas, showcase technological advances, and discuss research experiences in solving the world’s most challenging problems in circuits and systems in general.

The whole event spans five days, featuring 6 keynote speeches, 8 invited talks, five tutorials, twenty-four oral sessions and three poster sessions as well as several co-located social events, including academic visits.

Finally, no conference will succeed without the strong support of its participants. I would like to thank all the authors and attendees for participating in the conference. I wish you have a stimulating and fruitful time at the symposium, and memorable experience in Chengdu, China.

The Organization Committees, APCCAS 2018 & PrimeAsia 2018
Chengdu, China
Organizing Committees

APCCAS 2018

General Chair
Ming Liu, Chinese Academy of Sciences, China

General Co-Chairs
Xiaoyang Zeng, Fudan University, China
Chip-Hong Chang, Nanyang Technological University, Singapore

TPC Co-Chairs
Qiang Li, University of Electronic Science and Technology of China, China
Zhangming Zhu, Xidian University, China

Special Session Chair
Letian Huang, University of Electronic Science and Technology of China, China
Tong Zhang, South China University of Technology, China

Tutorial Chair
Xiong Zhou, University of Electronic Science and Technology of China, China

PrimeAsia 2018

General Chair
Qiang Li, University of Electronic Science and Technology of China, China

General Co-Chairs
Yoshifumi NISHIO, Tokushima University, Japan
Amara AMARA, ICT4D Strategist, Terre des hommes foundation, Switzerland IEEE
CASS President-Elect

TPC Chair
Ce Zhu, University of Electronic Science and Technology of China, China

Publicity Chair
Letian Huang, University of Electronic Science and Technology of China, China
Useful Information

Conference Venue

Shangri-La Hotel, Chengdu
Address: 9 Binjiang Dong Road, Chengdu, 610021, China
(Phone: (86 28) 8888 9999; Email: slcd@shangri-la.com)
**Free Wifi access is available for all delegates in the conference venue.**

Weather

Average Temperature in October in Chengdu

13℃ - 17℃

Bank and Foreign Exchange

The Currency is CNY here. You can exchange foreign currency 24hours at the airport, or exchange at the bank, Money exchanger.

Attention Please

Please take care of your belongings in the public places. Don’t stay too late in the city, don’t be alone in the remote area. Be aware of the strangers who offer you service, signature of charity, etc., at many scenic spots. You can search more Tourist Information and Security tips online.

Emergency

Ambulance: 120
Police: 110
Fire: 119
Instructions for Presentation

No-Show Policy
A paper not presented or presented by a non-author without prior written approval by the Conference Technical Program Chair will be removed from the final conference proceedings before uploading to IEEE Xplore®. No refund will be made to authors of those papers.
In case any absence or some presentations are less than 18 minutes, please come before your session starts.
*A best presentation will be selected from each session which will be announced and awarded an excellent oral presentation certificate at the end of this session.

Devices Provided by the Conference Organizer
Laptops (with MS-Office & Adobe Reader)
Projectors & Screen
Laser Sticks

Materials Provided by the Presenters
Oral Presentation: PowerPoint or PDF files. Please copy your slide file to the desktop before session starts
Poster Presentation: 1.8m high and 0.8m wide, portrait direction, punching around the four corners, suitable with Portal frame. During your poster session, the author should stay by your poster paper to explain and discuss your paper within visiting.

Duration of Each Presentation
Regular Oral Session: about 18-20 Minutes of Presentation including Q&A.
Keynote Speech: 40 Minutes of Presentation including Q&A.

About Dress Code
All participants are required to dress formally. Casual wear is unacceptable.
National formal dress is acceptable.
Best Paper Selection

One best paper will be selected by the TPC Committee from each APCCAS and PrimeAsia. The awarded paper will be announced during the Conference Banquet on Oct 28, 2018.

Student Travel Grants

We provide partial travel support to student speakers attending the conference. If selected and granted, the student will receive the support during the conference. This opportunity is sponsored by the IEEE Circuits and Systems Society.

YP & WiCAS Session

The YP (Young Professionals) special session aims at bringing together a panel of distinguish professionals, in the area of circuits and systems, and an attendance of young professionals and PhD students. The knowledge and expertise in Circuits, Systems, Signals, Modeling, Analysis, and Design can have a decisive impact on important issues such as Sustainable Energy, Bio-Health, Green Information Technology, Nano-Technology, and Scalable Information Technology Systems in the future. The invited speakers will share their thoughts and experience on building a professional career in the area of circuits and systems, by highlighting challenges and also by anticipating future opportunities. Women in Circuits and Systems (WiCAS) supports career development for IEEE CASS members, particularly women, minorities, and those at early career stages. The CAS Society welcome not only YP and WiCAS members but also all the APCCAS and PrimeAsia attendees to this session.

Academic Visiting

All attendees are welcome to have the Academic Visiting in Electronic Science and Technology Museum in UESTC, more details please refer to page 54.
## Conference Agenda

### October 26, 2018 - Friday

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<thead>
<tr>
<th>Time</th>
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<tbody>
<tr>
<td>10:30-18:00</td>
<td><strong>Registration and Reception</strong> at Hotel First Floor (Shangri-La Hotel)</td>
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<tr>
<td>14:00-18:00</td>
<td><strong>Tutorial 1</strong></td>
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<tr>
<td></td>
<td>[Room: Longquan]</td>
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<tr>
<td></td>
<td>General Design Flows and Examples of High-Speed SAR Type ADCs</td>
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<tr>
<td></td>
<td>by Yan Zhu &amp; Chi Hang Chan</td>
</tr>
<tr>
<td>14:00-17:00</td>
<td><strong>Tutorial 2</strong></td>
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<tr>
<td></td>
<td>[Room: Huanglong]</td>
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<tr>
<td></td>
<td>Internet of Things (IoT): Circuits, Architectures, Systems, and</td>
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<td></td>
<td>Demonstration</td>
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<tr>
<td></td>
<td>by Kiichi Niitsu</td>
</tr>
<tr>
<td>14:00-17:00</td>
<td><strong>Tutorial 3</strong></td>
</tr>
<tr>
<td></td>
<td>[Room: Kangding]</td>
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<tr>
<td></td>
<td>Design and Implementation for 5G Baseband Processing</td>
</tr>
<tr>
<td></td>
<td>by Ahmed Abdelgawad</td>
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<tr>
<td>14:00-15:30</td>
<td><strong>Tutorial 4</strong></td>
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<tr>
<td></td>
<td>[Room: Wangjiang]</td>
</tr>
<tr>
<td></td>
<td>Self-Powered and Energy-Autonomous CMOS Biomedical IoT design for</td>
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<td></td>
<td>Personalized Health Care Systems</td>
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<tr>
<td></td>
<td>by Chuan Zhang &amp; Xiaosi Tan</td>
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<tr>
<td>16:00-18:00</td>
<td><strong>Tutorial 5</strong></td>
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<tr>
<td></td>
<td>[Room: Wangjiang]</td>
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<tr>
<td></td>
<td>Large Signal and Small Signal Analysis in Analog Circuits</td>
</tr>
<tr>
<td></td>
<td>by Jinda Yang</td>
</tr>
<tr>
<td>18:30-20:00</td>
<td><strong>Welcome Reception</strong></td>
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<td>[Room: Jiuzhai &amp; Hongyuan]</td>
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### Morning Schedule - October 27, 2018 – Saturday

<table>
<thead>
<tr>
<th>Time</th>
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<tbody>
<tr>
<td>08:00-18:00</td>
<td><strong>Registration and Reception</strong> at Hotel First Floor</td>
</tr>
<tr>
<td>08:45-09:00</td>
<td><strong>Opening Ceremony</strong></td>
</tr>
<tr>
<td></td>
<td>Opening Remarks &amp; TPC Chair Address</td>
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# Conference Agenda

<table>
<thead>
<tr>
<th>Time</th>
<th>Session Title</th>
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<tbody>
<tr>
<td>09:00 - 09:40</td>
<td><strong>Keynote Speech 1</strong>&lt;br&gt;Developing Status and Trend for Nonvolatile Memory&lt;br&gt;by Ming Liu</td>
</tr>
<tr>
<td>09:40 - 10:20</td>
<td><strong>Keynote Speech 2</strong>&lt;br&gt;Energy Efficient System Architecture for Devices in Artificial Intelligence of Things&lt;br&gt;by Yong Lian</td>
</tr>
<tr>
<td>10:20 - 10:50</td>
<td><strong>Coffee Break</strong></td>
</tr>
<tr>
<td>10:50 - 11:30</td>
<td><strong>Keynote Speech 3</strong>&lt;br&gt;Next-Generation Energy-Efficient Computing for IoT and AI Chips: How to Overcome the Memory Wall&lt;br&gt;by Meng-Fan Chang</td>
</tr>
<tr>
<td>11:30 - 12:10</td>
<td><strong>Keynote Speech 4</strong>&lt;br&gt;AI and Intelligent IC Design/Manufacturing&lt;br&gt;by David Z. Pan</td>
</tr>
</tbody>
</table>

## Afternoon Schedule - October 27, 2018 – Saturday

<table>
<thead>
<tr>
<th>Time</th>
<th>Session Title</th>
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</thead>
<tbody>
<tr>
<td>14:00 - 15:30</td>
<td><strong>Parallel Session 1</strong>&lt;br&gt;[Room: Huanglong]&lt;br&gt;[1-AMSCS] Analog and Mixed-Signal Circuits and Systems&lt;br&gt;Papers: 15, 20, 24, 30, 40</td>
</tr>
<tr>
<td>14:00 - 15:30</td>
<td><strong>Parallel Session 2</strong>&lt;br&gt;[Room: Longquan]&lt;br&gt;[2-DCS] Digital Circuits and Systems&lt;br&gt;Papers: 47, 87, 184, 194, 214</td>
</tr>
<tr>
<td>14:00 - 15:30</td>
<td><strong>Parallel Session 3</strong>&lt;br&gt;[Room: Kangding]&lt;br&gt;[3-CCS] Communication Circuits and Systems&lt;br&gt;Papers: 23, 28, 34, 39, 166</td>
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# Conference Agenda

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<th>Event</th>
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<th>Location</th>
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<tbody>
<tr>
<td>15:30 - 16:00</td>
<td>Coffee Break &amp; Poster Session 1</td>
<td></td>
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</tr>
<tr>
<td>Papers: 178, 196, 206, 212, 279, 292, 311</td>
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<tr>
<td>16:00 - 18:00</td>
<td>Parallel Session 5</td>
<td>Huanglong</td>
<td>AMSCS</td>
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<tr>
<td>Papers: 86, 97, 105, 180, 185, 305</td>
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<tr>
<td>16:00 - 18:00</td>
<td>Parallel Session 6</td>
<td>Longquan</td>
<td>DCS</td>
</tr>
<tr>
<td>Papers: 32, 48, 189, 203, 290, 315</td>
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<tr>
<td>16:00 - 18:00</td>
<td>Parallel Session 7</td>
<td>Kangding</td>
<td>CCS</td>
</tr>
<tr>
<td>Papers: 172, 192, 314, 320, 321, 322</td>
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<tr>
<td>16:00 - 18:00</td>
<td>Parallel Session 8</td>
<td>Wangjiang</td>
<td>NDHSI</td>
</tr>
<tr>
<td>Papers: 94, 107, 181, 298, 299, 313</td>
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## Morning Schedule - October 28, 2018 – Sunday

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Room</th>
<th>Location</th>
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</thead>
<tbody>
<tr>
<td>08:00 - 18:00</td>
<td>Registration and Reception</td>
<td>Kangding &amp; Wangjiang</td>
<td></td>
</tr>
<tr>
<td>08:45 - 09:25</td>
<td>Keynote Speech 5</td>
<td></td>
<td>AMSCS</td>
</tr>
<tr>
<td>High Speed CMOS Analog-to-digital Converter Based Successive Approximation Register</td>
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<tr>
<td>by Zhangming Zhu</td>
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<tr>
<td>09:25 - 10:05</td>
<td>Keynote Speech 6</td>
<td></td>
<td>DCS</td>
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<tr>
<td>Globally Evolving Landscape for Innovations in Electronic Education</td>
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<tr>
<td>by Hannu Tenhunen</td>
<td></td>
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<tr>
<td>10:05 - 10:35</td>
<td>Coffee Break &amp; Poster Session 2</td>
<td></td>
<td>CCS</td>
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</tbody>
</table>
# Conference Agenda

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Room</th>
<th>Papers</th>
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<tbody>
<tr>
<td>10:35 - 12:05</td>
<td><strong>Parallel Session 9</strong></td>
<td>Kangding</td>
<td>9-AMSC Analog and Mixed Signal Circuits 13, 14, 33, 35, 36, 38, 89, 99</td>
</tr>
<tr>
<td>10:35 - 12:05</td>
<td><strong>Parallel Session 10</strong></td>
<td>Wangjiang</td>
<td>10-AMSCS Analog and Mixed-Signal Circuits and Systems 41, 43, 201, 209, 325</td>
</tr>
<tr>
<td>10:35 - 12:05</td>
<td><strong>Parallel Session 11</strong></td>
<td>Huanglong</td>
<td>11-DCS Digital Circuits and Systems 177, 116, 300, 2019, 294</td>
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### Afternoon Schedule - October 28, 2018 – Sunday

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<tr>
<th>Time</th>
<th>Session</th>
<th>Room</th>
<th>Papers</th>
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<tbody>
<tr>
<td>12:10 - 14:00</td>
<td><strong>Committee Meeting</strong></td>
<td>Kangding</td>
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<tr>
<td>14:00 - 16:00</td>
<td><strong>Parallel Session 13</strong></td>
<td>Kangding</td>
<td>13-DSP Digital Signal Processing 7, 100, 266, 267, 334</td>
</tr>
<tr>
<td>14:00 - 16:00</td>
<td><strong>Parallel Session 14</strong></td>
<td>Wangjiang</td>
<td>14-AMSCS Analog and Mixed-Signal Circuits and Systems 11, 183, 187, 199, 304, 333</td>
</tr>
<tr>
<td>14:00 - 16:00</td>
<td><strong>Parallel Session 15</strong></td>
<td>Huanglong</td>
<td>15-DA Design Automation 4, 19, 49, 117, 170, 200</td>
</tr>
<tr>
<td>14:00 - 16:00</td>
<td><strong>Parallel Session 16</strong></td>
<td>Longquan</td>
<td>16-BHCS Biomedical and Healthcare Circuits and Systems 42, 84, 167, 270, 293, 309</td>
</tr>
<tr>
<td>Time</td>
<td>Event</td>
<td>Location</td>
<td>Papers</td>
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<tr>
<td>16:00 - 16:30</td>
<td><strong>Coffee Break &amp; Poster Session 3</strong></td>
<td></td>
<td>102, 106, 110, 112, 169, 174, 175, 310</td>
</tr>
<tr>
<td>16:20 - 17:50</td>
<td><strong>YP&amp;WiCas Session</strong></td>
<td>[Room: Kangding &amp; Wangjiang]</td>
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<tr>
<td>18:00 - 20:30</td>
<td><strong>Banquet</strong></td>
<td>[Room: Jinguang Cheng]</td>
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### October 29, 2018 - Monday

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Location</th>
<th>Papers</th>
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<tbody>
<tr>
<td>08:00 - 12:00</td>
<td><strong>Registration and Reception</strong></td>
<td>at Hotel First Floor</td>
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<tr>
<td>08:40 - 10:10</td>
<td><strong>Parallel Session 17</strong></td>
<td>[Room: Kangding]</td>
<td>17-NNNE Neural Networks and Neuromorphic Engineering 25, 50, 51, 179, 316</td>
</tr>
<tr>
<td>08:40 - 10:10</td>
<td><strong>Parallel Session 18</strong></td>
<td>[Room: Wangjiang]</td>
<td>18-SSE2 Reconfigurable Architecture for Future Intelligent Systems 37, 46, 168, 271, 323</td>
</tr>
<tr>
<td>08:40 - 10:10</td>
<td><strong>Parallel Session 19</strong></td>
<td>[Room: Huanglong]</td>
<td>19-SSE3 Smart and Secure Integrated Systems for Autonomous Vehicles 93, 288, 289, 291, 295, 329</td>
</tr>
<tr>
<td>08:40 - 10:10</td>
<td><strong>Parallel Session 20</strong></td>
<td>[Room: Longquan]</td>
<td>20-SSE4 Hardware Security and Hardware Implementation of Post-Quantum Cryptography 263, 264, 272, 281, 285, 286</td>
</tr>
<tr>
<td>10:10 - 10:30</td>
<td><strong>Coffee Break</strong></td>
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<tr>
<td>10:30 - 12:00</td>
<td><strong>Parallel Session 21</strong></td>
<td>[Room: Kangding]</td>
<td>21-SSE1 Emerging threats in the IoT era: chip reliability and security 114, 115, 208, 307, 318</td>
</tr>
<tr>
<td>10:30 - 12:00</td>
<td><strong>Parallel Session 22</strong></td>
<td>[Room: Wangjiang]</td>
<td>22-SSE6 Future Circuits and Systems based on Emerging</td>
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Memory Technologies

**Papers:** 95, 273, 282, 283, 326, 337

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<tbody>
<tr>
<td>10:30 - 12:00</td>
<td><strong>Parallel Session 23</strong></td>
<td>Huanglong</td>
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<tr>
<td></td>
<td>[23-SSE7] Design and Implementation for Advanced Baseband Signal Processing</td>
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<td></td>
<td><strong>Papers:</strong> 297, 319, 330, 331, 332</td>
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<tr>
<td>10:30 - 12:00</td>
<td><strong>Parallel Session 24</strong></td>
<td>Longquan</td>
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<tr>
<td></td>
<td>[24-SSE5] Artificial Intelligent (AI) System and Advanced Processing (AP) Core Technology</td>
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<td><strong>Papers:</strong> 269, 280, 296, 306, 284, 287</td>
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<th>Time</th>
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<tbody>
<tr>
<td>14:00 - 17:30</td>
<td><strong>Academic Visiting</strong></td>
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**October 30, 2018 - Tuesday**

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<th>Time</th>
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<tbody>
<tr>
<td>09:00 - 17:30</td>
<td><strong>One Day Tour</strong></td>
</tr>
<tr>
<td>14:00 - 17:30</td>
<td><strong>Academic Visiting</strong></td>
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</tbody>
</table>
Developing Status and Trend for Nonvolatile Memory
Ming Liu
Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS), China

Biography: Ming Liu received the B.S. and M.S. degrees in semiconductor physics and device from Hefei Polytechnic University, Hefei, China, in 1985 and 1988, respectively, and the Ph.D. degree in microelectronics from Beijing University of Aeronautics and Astronauts, China, in 1998. From 1998 to 1999, she was a Postdoctoral Scholar in the Chinese Academy of Sciences (CAS). She joined the Institute of Microelectronics, CAS, in 2000. She is currently the Director of the Key Laboratory of Nanofabrication and Novel Devices Integration Technology and the Key Laboratory of Microelectronics Devices and Integrated Technology. She was selected as an Academician of Chinese Academy of Sciences and IEEE Fellow in 2015 and 2018 separately. Her research interests are semiconductor materials, integrated circuit processing, nanofabrication, nano-electronics, molecular electronics, and non-volatile memory.

Abstract: The common memory technologies used in the traditional memory hierarchy, are increasingly constrained by fundamental technology limits. The increasing leakage power for SRAM and refresh dynamic power for DRAM has posed challenges to circuit and architecture designers. Emerging memory technologies such as spin transfer torque RAM (STT-RAM), phase-change RAM (PCRAM), and resistive RAM (RRAM) are being explored as potential alternatives to existing memories in future computing systems. Especially, due to the excellent compatibility with CMOS process and ease of 3D integration, RRAM provides a promising potential for embedded and standalone application. In this talk, current status of RRAM technology will be discussed, including switching mechanism, array architecture, 3D integration, target applications,
challenges and future trends. A new era of convolutional computer architectures could be expected after the mature of emerging new NVM technologies.

Keynote Speaker 1-2

09:40-10:20, Day 2, October 27, 2018 [Jinguan Cheng (First Floor) ]

Energy Efficient System Architecture for Devices in Artificial Intelligence of Things
Yong Lian
Fellow of Academy of Engineering Singapore, Fellow of IEEE; President, IEEE Circuits and Systems Society; Member, IEEE Fellow Committee

Biography: Dr. Yong Lian received the B.Sc degree from the College of Economics & Management of Shanghai Jiao Tong University in 1984 and the Ph.D degree from the Department of Electrical Engineering of National University of Singapore (NUS) in 1994. He worked in industry for more than 9 years before joining NUS in 1996. He was appointed as the first Provost's Chair Professor in the Department of Electrical and Computer Engineering of NUS in 2011. His research interests include low power techniques, continuous-time signal processing, biomedical circuits and systems, and computationally efficient signal processing algorithms. His research has been recognized with more than 20 awards including the 1996 IEEE Circuits and Systems Society's Guillemin-Cauer Award, the 2008 Multimedia Communications Best Paper Award from the IEEE Communications Society, 2011 IES Prestigious Engineering Achievement Award, 2012 Faculty Research Award, 2013 Outstanding Contribution Award from Hua Yuan Association and Tan Kah Kee International Society, 2014 Chen-Ning Yang Award in Science and Technology for New Immigrant, and the 2015 Design Contest Award in 20th International Symposium on Low Power Electronics and Design. He is also the recipient of the National University of Singapore Annual Teaching Excellence Awards in 2009 and 2010, respectively.

Dr. Lian is the President of the IEEE Circuits and Systems (CAS) Society, a member of IEEE Fellow Committee, a member of IEEE Biomedical Engineering
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Award Committee, a member of Steering Committee of the IEEE Transactions on Biomedical Circuits and Systems. He was the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II for two terms from 2010 to 2013. He served many positions in the IEEE CAS Society including Vice President for Publications, Vice President for Asia Pacific Region, Chair of the Biomedical Circuits and Systems Technical Committee, Chair of DSP Technical Committee, Distinguished Lecturer, etc. He is the founder of several conferences including BioCAS, ICGCS, and PrimeAsia.

Abstract: Internet-of-Things (IoT) is the inter-networking of physical devices, vehicles, buildings, and objects with embedded sensors. It is estimated that by 2020 there will be more than 34 billion IoT devices connected to the Internet. Nearly $6 trillion will be spent on IoT solutions over the next five years. Artificial Intelligence (AI), on the other hand, is intelligence demonstrated by machines that work and react like humans. Some examples of AI powered applications are voice-powered personal assistants like Siri and Cortana, machine translation, email spam filter, etc. The combination of AI and IoT gives birth of Artificial Intelligence of Things (AIoT). AIoT devices differ from IoT devices that not only they sense, store, transmit data but also analyze and act on data, i.e. the AIoT device makes a decision or perform a task similar to what a person could do. Most of existing “smart” IoT devices, which are controllable from an APP, are not AIoT devices. The true AIoT devices should be able to perform a task on your behalf, such as autonomous vehicle – it drives for you. The enabling technology for the AIoT device is embedded AI. This talk will cover low power techniques for embedded AI in AIoT applications. The focus is on the energy efficient system architecture that utilizes the brain-inspired event-driven signal representation. The event-driven signal representation enables data compression at the input source, which greatly reduces the power for data transmission and processing. We will show by examples that the event-driven system significantly improves energy efficiency and is well suited for AIoT applications.
Next-Generation Energy-Efficient Computing for IoT and AI Chips: How to Overcome the Memory Wall

Meng-Fan Chang
National Tsing Hua University, Taiwan
Professor, National Tsing Hua University (NTHU), Taiwan
Program Director, Microelectronics Program, Ministry of Science and Technology (MOST), Taiwan, 2018-2020
IEEE Distinguished Lecturer (DL), Circuits and System Society (CASS)

Biography: Dr. Chang is a full Professor in the Dept. of Electrical Engineering of National Tsing Hua University (NTHU), Taiwan. Dr. Chang obtained considerable practical experience before joining NTHU in 2006, having spent more than 10 years working in industry.
Between 1997 and 2006, Dr. Chang worked in the development of SRAM/ROM/Flash macros/compilers at Mentor Graphics (New Jersey, US), TSMC (Taiwan), and the Intellectual Property Library Company (Taiwan). His research interests include circuit design for volatile and nonvolatile memory, 3D-Memory, nonvolatile and spintronics logics, circuit-device-interactions in non-CMOS devices, memristor circuits, computing-in-memory and neuromorphic circuits for deep learning and artificial intelligent (AI) chips.
Since 2010, Dr. Chang has authored or co-authored more than 40+ top conference papers (including 14 ISSCC, 15 VLSI Symposia, 8 IEDM, and 5 DAC) as well as 40+ IEEE journal papers and 40+ US patents. He is an associate editor for IEEE TVLSI, and IEEE TCAD. He has been serving on technical program committees for ISSCC, IEDM (Executive committee, Chair of MT sub-committee), DAC, A-SSCC, IEEE CAS Society (Chair Elect of NG-TC), and numerous international conferences. He is a Distinguished Lecturer (DL) for IEEE Circuits and Systems Society (CASS) during 2017-2018. He is the recipient of several prestigious national-level awards in Taiwan, including the Outstanding Research Award of MOST-Taiwan, Outstanding Electrical Engineering Professor Award, Ta-You Wu Memorial Award, Academia Sinica Junior Research Investigators Award, Outstanding Chip Design Awards, and Golden Silicon Awards. He currently is the Program Director of the Microelectronics Program at the...
Ministry of Science and Technology (MOST) in Taiwan.

Abstract: Memory has proven a major bottleneck in the development of energy-efficient chips for IoT applications and artificial intelligence (AI). Recent memory devices not only serve as memory macros, but also enable the development of nonvolatile logics (nvLogics) and computing-in-memory (CIM) for IoT and AI chips. In this talk, we will review recent trend of IoT and AI chips. Then, we will examine some of the challenges, circuits-devices-interaction, and recent progress involved in the further development of SRAM, emerging memory (STT-MRAM, ReRAM and PCM), nvLogics and CIMs for IoT and AI chips.
Keynote Speaker 1-4

10:50-11:30, Day 2, October 27, 2018       [Jinguan Cheng (First Floor) ]

AI and Intelligent IC Design/Manufacturing

David Z. Pan
the University of Texas at Austin, United States

Biography: David Z. Pan (IEEE Fellow, SPIE Fellow) received his BS degree from Peking University and MS/PhD degrees from UCLA. He is currently Engineering Foundation Professor at the Department of Electrical and Computer Engineering, The University of Texas at Austin. His research interests include cross-layer IC design for manufacturing, reliability, security, machine learning in EDA, hardware acceleration, design/CAD for analog/mixed signal designs and emerging technologies such as nanophotonics. He has published over 320 refereed journal/conference papers and 8 US patents. He has served in many journal editorial boards and conference committees, including various leadership roles. He has received many prestigious awards, including SRC Technical Excellence Award, 16 Best Paper Awards, DAC Top 10 Author Award in Fifth Decade, ASP-DAC Frequently Cited Author Award, Communications of ACM Research Highlights, ACM/SIGDA Outstanding New Faculty Award, NSF CAREER Award, IBM Faculty Award (4 times), UCLA Engineering Distinguished Young Alumnus Award, UT Austin RAISE Faculty Excellence Award, and many international CAD contest awards, among others. His students have also won many awards, including the First Place of ACM Student Research Competition Grand Finals in 2018, ACM/SIGDA Student Research Competition Gold Medal (twice), ACM Outstanding PhD Dissertation in EDA (twice), EDAA Outstanding Dissertation Award, and so on.

Abstract: Artificial intelligence (AI) studies the theory and development of computing systems able to learn, reason, act and adapt. Integrated circuit (ICs), powered by the semiconductor technology, enable all modern computing systems with amazing level of integration, e.g., a small chip (<1cm2) nowadays can integrate billions of transistors. As the semiconductor technology enters the era of extreme scaling (1x nm), IC design and manufacturing complexities are
extremely high. Intelligent cross-layer design and manufacturing co-optimizations are in critical demand for better performance, power, yield, reliability, security, time-to-market, and so on. This talk will discuss the synergy between modern AI technologies (e.g., pattern recognition, machine learning, deep learning) with intelligent deep-nanoscale IC design and manufacturing. Several case studies will be presented on AI for IC, including advanced lithography modeling, hotspot detection, mask synthesis, physical design, and security. Meanwhile, customized ICs for AI can further improve the training and inference performance-energy efficiency by orders of magnitude. Thus, the co-evolution of AI algorithms and IC technologies shall be investigated jointly to enhance the research and development of each other.
Keynote Speaker 2-1

08:45-09:25, Day 3, October 28, 2018

High Speed CMOS Analog-to-digital Converter Based Successive Approximation Register

Zhangming Zhu
Xidian University, China

Biography: Prof. Zhangming Zhu (1978-) is currently a full Professor with the School of Microelectronics in Xidian University, Xi’an, China. He received the Ph.D. degrees in Microelectronics from the Xidian University, China, in 2004. Since 2004, he has been a lecturer of Xidian University. He was promoted to associate professor and full professor in 2005 and 2009, respectively, both with exceptional admission. In 2013, he was appointed as the Chief Professor (Director) of the Key Innovative Research Team of Shaanxi Province, China. He was the recipient of the National Science Fund for Distinguished Young Scholar and Excellent Young Scholar (selected by the National Natural Science Foundation of China), the New Century Excellent Talent in University (selected by the Ministry of Education of China).

Zhu’s research interests are broadly in the area of data converters and analog front end (AFE), IPD based TSV, RF-ICs. He has authored/coauthored over 100 papers in journal, including IEEE TCAS-I, IEEE TMTT, IEEE TIE, IEEE TPE, IEEE TCAS-II, IEEE TIM, IEEE MWCL, IEEE TVLSI, IEEE TED.

Abstract: Successive Approximation Register (SAR) analog-to-digital converters (ADCs) benefit from their simple configuration and mostly dynamic operation exhibiting excellent power and area efficiency under technology down scaling. The SAR architecture demands a stringent noise requirement for the comparator while aiming for high resolution. The signal-to-noise ratio (SNR) is usually dominated by the comparator’s thermal noise. The mismatch spurs due to the timing, offset and gain limit both signal-to-noise distortion ratio (SNDR) and spurious-free dynamic range (SFDR). In this talk, some key technique for high speed SAR-based ADCs will been discussed.
Globally Evolving Landscape for Innovations in Electronic Education

Hannu Tenhunen
Royal Institute of Technology (KTH), Stockholm, Sweden

Biography: Prof. Dr.h.c Prof.h.c. Hannu Tenhunen is chair professor of Electronic Systems at Royal Institute of Technology (KTH), Stockholm, Sweden. Prof. Tenhunen has held professor position as full professor, invited professor or visiting honorary professor in Finland (TUT, UTU), Sweden (KTH), USA (Cornel U), France (INPG), China (Fudan and Beijing Jiatong Universities), and Hong Kong (Chinese University of Hong Kong), and has an honorary doctorate from Tallinn Technical University.

He has been director of multiple national large scale research programs or being an initiator and director of national or European graduate schools. He has actively contributed on VLSI and SoC design in Finland and Sweden via creating new educational programs and research directions, most lately at European level as being the EU-level Education Director of the new European flagship initiative European Institute of Technology and Innovations (EIT), and its Knowledge and Innovation Community EIT ICT Labs. Prof. Tenhunen has been active in promoting the innovation system and innovation support mechanism in research and education both at national and European level. Prof. Tenhunen has been a board member in science parks, start-up companies, and has served as advisor or expert for high technology companies and venture capitalists, as well as evaluator for EU and national programs and research institutes. He has supervised over 70 M.Sc. thesis, 39 doctoral thesis, and 8 post-doc. From his doctoral students and post-docs, as of today, 21 are currently professors and associate professors.

Prof. Tenhunen has served in Technical Program Committee's of all major conferences in his area, have been general chairman or vice-chairman or member of Steering Committee of multiple conferences in his core competence areas. He has been one of the founding editorial board member of 3 scientific journal, have been quest editor for multiple special issues of scientific journals.
or books, and have contributed numerous invited papers to journals. He has contributed to over 127 journal papers, over 656 reviewed international conference papers, over 190 non-reviewed papers, local conference papers, or other publications, and 9 international patents granted in multiple countries. Prof. Tenhunen is member of Academy of Engineering Science of Finland

**Abstract:** One of the core fundamental changes transforming our societies and individual life is much larger utilization of electronics technologies on our daily lives. We have had a number of significant breakthrough covering the different phase of evolution: (i) the microprocessor era, (ii) the personal communication era with DSP optimized systems, (iii) the networked era with seaming less integration of technologies and applications, and most recently providing artificial intelligence and neuromorphic computing to masses. For the last item we can clearly recognize the race to the edge of global Internet-of-Things network with an aim to transferring the interconnected specialized sensors to a fog based computing platform.

In this overview presentation we will look the evolution of technology, transforming our educational profiles, as well as how we build up global partnerships in this domain. The key conclusion is that we need more immersive strategic co-operation between geographic areas as well as across industrial segments. Some examples will be provided on this based on European experience, e.g. through the European Institute of Innovation and Technology (EIT).
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General Design Flows And Examples Of High-Speed Sar Type Adcs
Time: 14:00-18:00

Yan Zhu, University of Macau, China
Yan Zhu (S’10- M’17) received the B.Sc. degree in electrical engineering and automation from Shanghai University, Shanghai, China, in 2006, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau Macao, China, in 2009 and 2011, respectively. She is now an assistant professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China. She received Best Paper award in ESSCIRC 2014, the Student Design Contest award in A-SSCC 2011, the Chipidea Microelectronics Prize and Macao Scientific and Technological R&D Awards in 2012, 2014 and 2016 for outstanding Academic and Research achievements in Microelectronics. She has published more than 50 technical journals and conference papers in her field of interests, and holds 3 US patents. Her research interests include low-power and wideband high-speed Nyquist A/D converters as well as digitally assisted data converter designs.

Chi Hang Chan, University of Macau, China
Chi-Hang Chan (S’12 M’15) was born in Macau S.A.R., China, in 1985. He received the B.S. degree in electrical engineering from University of Washington (U.W. Seattle), USA, in 2008, the M.S. and Ph.D. degree from the University of Macau, Macao, China, in 2012 and 2015, respectively, where he currently serves as assistant professor. He was an intern with Chipidea Microelectronics (Now Synopsys), Macau, during his undergraduate studies. He received the Chipidea Microelectronics Prize and Macau Science and Technology Development Fund (FDCT) Postgraduates Award (Master Level) in 2012 and 2011, respectively. He also received Macau FDCT Award for Technological Invention (2nd class) as well as Macao Scientific and Technological R&D for Postgraduates Award (Ph.D. Level) in 2014 for outstanding Academic and Research achievements in Microelectronics. He is the recipient of the 2015 Solid-State-Circuit-Society (SSCS) Pre-doctoral Achievement Award. He also is the co-recipient of the 2011 ISSCC Silk Road Award and Student Design Contest Award in A-SSCC 2011. His research interests include Nyquist ADC and mixed signal circuits. Currently, his research mainly focuses on the comparator offset calibration, Flash and Multi-bit SAR ADC.
**Abstract:** This tutorial will address the comprehensive top-to-bottom design methodologies and considerations for modern High Performance ADCs in Nano CMOS. It is divided into two sub-sessions to introduce the practical design methodologies, considerations with multiple examples for ADC designs. In the first session, the SAR-SAR sub-ranging ADC architecture’s general design flows and considerations based on noise budget will be discussed. The session two covers another design example of Multi-bit SAR ADC. Some design issues of different comparator architectures, offset calibrations and comparator metastability will be introduced.

After this two-half day tutorial, the audiences will get the general design knowledge of how to design a SAR based ADC and will be able to understand the key driving forces for the latest developments and most important design considerations and techniques for high speed SAR type ADCs.

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**Self-Powered and Energy-Autonomous CMOS biomedical IoT design for personalized health care systems**

**Time:** 14:00-17:00

[Room: Huanglong]

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**Kiichi Niitsu, Nagoya University, Japan**

Kiichi Niitsu (S’05-M’10) was born in Japan, in 1983. He received the B.S. degree summa cum laude, M.S. and Ph.D. degrees in electrical engineering from Keio University, Yokohama, Japan, in 2006, 2008, and 2010, respectively. From 2010, he was an Assistant Professor at Gunma University, Kiryu, Japan. From 2012, he was a Lecturer at Nagoya University, Nagoya, Japan. Since 2016, he is currently an Associate Professor at Nagoya University, Nagoya, Japan. Since 2015, he serves concurrently as Precursory Research for Embryonic Science and Technology (PRESTO) researcher, Japan Science and Technology Agency (JST). His current research interest lies in the low-power and high-speed technologies of analog and digital VLSI circuits for biomedical application.

From 2008 to 2010, Dr. Niitsu was a Research Fellow of the Japan Society for the Promotion of Science (JSPS), a Research Assistant of the Global Center of Excellence (GCOE) Program at Keio University and a Collaboration Researcher of the Keio Advanced Research Center (KARC).

He was awarded the 2006 KEIO KOUGAKUKAI Award, the 2007 INOSE Science Promotion Award, the 2008 IEEE SSCS Japan Chapter Young Researcher Award and
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the 2009 IEEE SSCS Japan Chapter Academic Research Award both from IEEE Solid-State Circuits Society Japan Chapter, the 2008 FUJIWARA Award from the FUJIWARA foundation, 2011 YASUJIRO NIWA Outstanding Paper Award, 2011 FUNAI Research Promotion Award, 2011 Ando Incentive Prize for the Study of Electronics, 2011 Ericsson Young Scientist Award, 2012 ASP-DAC University LSI Design Contest Design Award, NF Foundation R&D Encouragement Award, AKASAKI Award from Nagoya University, IEEE Nagoya Section Young Researcher Award, IEEE Biomedical Circuits and Systems Conference 2016 (BioCAS 2016) Best Paper Award, and the 2017 Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology, the Young Scientists' Prize.

He has published 54 referred original journal papers, 114 international conference papers, and 3 book chapters including 3 TBioCAS, 1 TCAS-I, 1 TCAS-II, 5 JSSC, 5 TVLSI, 9 BioCAS, 1 ISCAS, 2 ICECS, 7 APCCAS, 2 ISSCC, 4 Symp. on VLSI Circuits, 4 A-SSCC. He served as a technical committee of IEEE biomedical circuits and systems (BioCAS TC), a Review Committee Member of ISCAS 2017/2018, a Technical Program Committee of ICECS 2018, a Review Committee Member of APCCAS 2014, an editorial committee of IEICE Transactions on Electronics, Special Section on Analog Circuits and Related SoC Integration Technologies, and an editorial committee of IEICE ESS Fundamental Review. He is a member of IEEE, IEICE (the Institute of Electronics, Information and Communication Engineers of Japan), and JSAP (the Japan Society of Applied Physics).

Abstract: CMOS Biosensor is promising enabler for next-generation biomedical IoTs for personalized health care systems. This tutorial introduces CMOS biomedical IoT design from fundamental to state-of-the-art.

First, the tutorial introduces the fundamental of CMOS biosensors. Operational mechanism and applications of each types of CMOS biosensors such as potentiometric, amperometric, impedimetric, and ISFET are summarized.

Latter part introduces development of energy-autonomous biomedical IoTs. Ensuring stable energy is one of the most important current challenges in wearable and implantable biomedical systems. For addressing this issue, many developments with respect to batteries, wireless power delivery, and energy harvesting have been reported. One of the promising candidates is bio fuel cell. In this tutorial, the fundamental and forecast of the bio-fuel-cell-operated biosensing systems. Firstly, I will summary the fundamental basics of bio fuel cell including operation mechanism, its performance, and its advantages/disadvantages. Secondary, I will introduce the examples of the bio-fuel-cell-operated biosensing
systems. Thirdly, I will introduce the supply-sensing architecture presented in BioCAS 2015/2016 from our group. The supply-sensing architecture uses bio-fuel cells as both power source and sensing converter. In addition, I will plan to present the latest result on the work on Glucose-fuel-cell-operated Glucose sensing system which can be applied to self-powered continuous Glucose monitoring system (CGMS). The tutorial will conclude with a discussion of recent work and future applications on the bio-fuel-cell-operated biosensing systems.

Internet of Things (IoT): Circuits, Architectures, Systems, and Demonstration
Time: 14:00-17:00  
[Room: Kangding]

Ahmed Abdelgawad, Central Michigan University, USA

Dr. Ahmed Abdelgawad received his M.S. and Ph.D. degree in Computer Engineering from University of Louisiana at Lafayette in 2007 and 2011 and subsequently joined IBM as a Design Aids & Automation Engineering Professional at Semiconductor Research and Development Center. In Fall 2012 he joined Central Michigan University as a Computer Engineering Assistant Professor. In Fall 2017, Dr. Abdelgawad was early promoted as a Computer Engineering Associate Professor. His area of expertise is distributed computing for Wireless Sensor Network (WSN), Internet of Things (IoT), Structural Health Monitoring (SHM), data fusion techniques for WSN, low power embedded system, video processing, digital signal processing, Robotics, RFID, Localization, VLSI, and FPGA design. He has published two books and more than 65 articles in related journals and conferences. Dr. Abdelgawad served as a reviewer for several conferences and journals, including IEEE W-F-IoT, IEEE ISCAS, IEEE SAS, Springer, Elsevier, IEEE Transactions on VLSI, and IEEE Transactions on I&M. He severed in the technical committees of IEEE ISCAS 2007, IEEE ISCAS 2008, and IEEE ICIP 2009 conferences. He served in the administration committee of IEEE SiPS 2011. Dr. Abdelgawad has been appointed as a Track Chair of the International Conference on Cognitive and Sensor Networks (MIC-CSN 2013). He also served in the organizing committee of ICECS2013 and 2015 IEEE ICECS2015. Dr. Abdelgawad is the publicity chair in North America of the IEEE WF-IoT 2016/18 conferences. He is the finance chair of the IEEE ICASSP 2017. He is the TPC Co-Chair of IoT International Innovation Conference 2017 (I3C’17), the TPC Co-Chair of Global Internet of Things Summit (GIoTS 2017), and the technical program chair of IEEE MWSCAS 2018. He is currently the IEEE
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Northeast Michigan section chair and IEEE SPS Internet of Things (IoT) SIG Member. In addition, Dr. Abdelgawad served as a PI and Co-PI for several funded grants from NSF.

Abstract: Internet of Things (IoT) is the network of physical objects or "things" embedded with electronics, software, sensors, and network connectively. It enables the objects to collect, share, and analyze data. The IoT has become an integral part of our daily lives through applications such as public safety, intelligent tracking in transportation, industrial wireless automation, personal health monitoring, and health care for the aged community. IoT is one of the latest technology that will change our lifestyle in coming years. Experts estimate that as of now, there are 25 billion connected devices, and by 2020 it would reach to 50 billion devices. This tutorial aims to introduce the design and implementation of IoT systems. The foundations of IoT will be discussed throughout real applications. Challenges and constrains for the future research in IoT will be discussed. In addition, research opportunities and collaboration will be offered for the attendees.

Design and Implementation for 5G Baseband Processing
Time: 14:00-15:30  [Room: Wangjiang]

Chuan Zhang, Southeast University, China

Chuan Zhang is now an associate professor of National Mobile Communications Research Laboratory, School of Information Science and Engineering, Southeast University, Nanjing, China. He received B.E. degree (summa cum laude) in microelectronics and M.E. degree (summa cum laude) in VLSI design from Nanjing University, Nanjing, China, in 2006 and 2009, respectively. He received both M.S.E.E. degree and Ph.D. degree in Department of Electrical and Computer Engineering, University of Minnesota, Twin Cities (UMN), USA, in 2012. His current research interests include low-power high-speed VLSI design for digital signal processing and digital communication, bio-chemical computation and neuromorphic engineering, and quantum communication. Dr. Zhang is a member of Seasonal School of Signal Processing (S3P) and Design and Implementation of Signal Processing Systems (DISPS) TC of the IEEE Signal Processing Society; Circuits and Systems for Communications (CASCOM) TC, VLSI Systems and Applications (VSA) TC, and Digital Signal Processing (DSP) TC of IEEE Circuits and
Dr. Zhang received the Excellent Bachelor Dissertation Award of Nanjing University in 2006, and the Excellent Master Dissertation Award of Jiangsu Province in 2009. He received the Three-Year University-Wide Graduate School Fellowship of UMN in 2009, and Doctoral Dissertation Fellowship of UMN in 2012. He has been selected by the first Innovative and Entrepreneurial Doctoral Talent Program of Jiangsu Province in 2014, Outstanding Young Faculty Teaching and Research Support Program of Southeast University in 2016, and the first Young Scientific Talent Lift Program of Jiangsu Province in 2017. He received the Leike Excellence in Teaching Award of Southeast University in 2016, the Qingyun Sun Excellence in Teaching Award of Southeast University in 2017, and the University-Wide Excellence in Teaching Award of Southeast University in 2017.


**Xiaosi Tan, Southeast University, China**

Xiaosi Tan is currently research fellow in National Mobile Communications Research Laboratory, School of Information Science and Engineering, Southeast University, Nanjing, China. She received the B.S. degree in applied mathematics from Beijing University of Technology, Beijing, China, in 2009, and the Ph.D. degree in mathematics from Texas A&M University, College Station, Texas, USA, in 2015. Her current research interests include emerging technologies for 5G cellular...
networks, including machine learning for wireless networks, massive MIMO and massive MTC communications.

**Abstract:** This tutorial focuses on Advanced Baseband Processing Circuits and Systems for 5G Communications: an emerging research field enabling 5G from theory to practice. By committing itself to the emerging techniques of baseband processing circuits and systems for 5G, this tutorial means to bring a synthesized source and wide view of recent progress and existing challenges in this particular but very important research area, including: 1) algorithm and code construction for 5G baseband processing; 2) algorithm and implementation co-design; 3) architecture and implementation optimization for 5G baseband; and 4) artificial intelligence (AI) for 5G baseband. The tutorial will identify technical challenges and recent results related to DISPS applications to 5G scenarios such as Internet of Things, Autonomous Vehicles, Robotics and UAVs, and Smart Buildings and Cities.

**Large Signal and Small Signal Analysis in Analog Design**

**Time:** 16:00-18:00

**[Room: Wangjiang]**

**Jinda Yang, 3PEAK INC., China**

Jinda Yang received bachelor degree from USTC (University of Science and Technology of China) in 2007 and master degree from Fudan University in 2011. He worked at HiSilicon for over 7 years, where he design high performance ADC for wireless base station and ultrahigh speed ADC for ODSP. He holds 10 Chinese patents and 4 US patents in the ADC field.

**Abstract:** Large signal and small signal responses are two closely related aspects of an analog system. These two characteristics usually correspond to circuits’ nonlinearity and stability, respectively. They are the main concerns of designing circuits in signal chain. By expanding the transfer function $f(x)$ of an analog system into Taylor series, the first term is the DC operating point, the second term is the linear term concerned with the small signal analysis, while the other high order terms are nonlinear terms which can be investigated by large signal analysis.

This tutorial will introduce the basic theory and intuitive analysis of zeros and poles in small signal response with some examples of practical circuits. Origin of nonlinearity and its influence will be introduced. What’s more, linearization techniques in large signal response will be illustrated.
AMSCS: Analog and Mixed-Signal Circuits and Systems
Session Chair: Quanzhen Duan, Tianjin University of Technology, China
Time: 14:00-15:30 [Room: Huanglong]

15  Title: High-Resolution PPM for Time-Based Architectures
       Authors: Mostafa Rashdan
       Affiliation: The American University of the Middle East, Kuwait

20  Title: Low-Voltage Bandgap Reference Circuit in 28nm CMOS
       Authors: Zhanke Yan, Chunming Zhang and Menghai Wang
       Affiliation: Xi'an University of Posts & Telecommunications, China

24  Title: An 11b 80MS/s SAR ADC With Speed-Enhanced SAR Logic and
       High-Linearity CDAC
       Authors: Yuefeng Cao, Yongzhen Chen, Zhekan Ni, Fan Ye and Junyan Ren
       Affiliation: State Key Laboratory of ASIC and System, Fundan University,
       Shanghai, China

30  Title: A Standard-cell Based A/D Converter with Back-gate VCO and Fat Tree
       Encoder
       Authors: Tokuya Fukuyama, Takao Kihara and Tsutomu Yoshimura
       Affiliation: Osaka Institute of Technology, Japan

40  Title: A Compact Bulk-Driven Four-Quadrant Analog Multiplier in Weak
       Inversion
       Authors: Prajuab Pawarangkoon and Chutham Chutham
       Affiliation: Mahanakorn University of Technology, Thailand
DCS: Digital Circuits and Systems
Session Chair: Weiwei Shi, Shenzhen University, China
Time: 14:00-15:30 [Room: Longquan]

47  Title: An Area Efficient True Random Number Generator Based on Modified Ring Oscillators
    Authors: Mehmet Alp Şarkışla and Salih Ergün
    Affiliation: TUBİTAK, Turkey

87  Title: A High-Throughput Real-Time Prewitt Operator on Embedded NEON+ARM System
    Authors: Lin Chenxi¹, Qian Hui¹ and Wang Zhongfeng²
    Affiliation: 1. Fuzhou University, China
               2. Nanjing University, China

184 Title: 40-nm 2xVDD Digital Output Buffer Design With DDR4-Compliant Slew Rate
    Authors: Chua-Chin Wang, Zong-You Hou and Ssu-Wei Huang
    Affiliation: National Sun Yat-Sen University, Taiwan

194 Title: Low-Cost Approximate Multiplier Design using Probability-Driven Inexact Compressors
    Authors: Yi Guo, Heming Sun, Li Guo and Shinji Kimura
    Affiliation: Waseda University, Japan

214 Title: A Disturb-Free 10T SRAM Cell with High Read Stability and Write Ability for Ultra-Low Voltage Operations
    Authors: Jiubai Zhang, Yajuan He and Xiaoqing Wu
    Affiliation: University of Science and Technology of China, China
Day 2, Saturday, October 27, 2018

PARALLEL SESSION 3

CCS: Communication Circuits and Systems
Session Chair: Le Ye, Peking University, China
Time: 14:00-15:30 [Room: Kangding]

23 Title: Application of novel architectures for Modulation Recognition
Authors: Yujie Sang and Li Li
Affiliation: Chengdu University of Information Technology, China

28 Title: A Polyphase Decimation Filter for Time-Interleaved ADCs in Direct-RF Sampling Receivers
Authors: Yuma Isobe, Takao Kihara and Tsutomu Yoshimura
Affiliation: Osaka Institute of Technology, Japan

34 Title: A ZVS Active Rectifier with Adaptive On/Off Delay Compensation for WPT Systems
Authors: Yanzhao Ma, Kai Cui and Zhengjie Ye
Affiliation: Research & Development Institute of Northwestern Polytechnical University in Shenzhen, China

39 Title: A Current Reuse Wideband LNA with Complementary Noise and Distortion Cancellation for Ultrasound Imaging Applications
Authors: Yuxuan Tang, Yulang Feng, Qingjun Fan and Jinghong Chen
Affiliation: University of Houston, USA

166 Title: Study of mutual injection pulling in a 5-GHz, 0.18-μm CMOS cascaded PLL
Authors: Kazuki Miyao, Tatsuya Okafuji, Takao Kihara and Tsutomu Yoshimura
Affiliation: Osaka Institute of Technology, Japan
PARALLEL SESSION 4

PEDCS: Power/Energy Devices, Circuits and Systems
Session Chair: Ping Luo, University of Science and Technology of China
Time: 14:00-15:30  [Room: WangJiang]

108  Title: Effect of Control Delay on Small Signal Model for Buck Converter with
     Constant on Time Control
     Authors: Mingyu Yang, Shaowei Zhen and Sunze Zhou
     Affiliation: UESTC, China

113  Title: Fully Integrated High-Voltage Level Shifts and Drivers for Buck
     Converters
     Authors: Junxiao Chen and Lenian He
     Affiliation: Zhejiang University, China

202  Title: A Chip-Area-Efficient Subthreshold CMOS Voltage Reference with High
     PSRR Based on Compensated DVGS of NMOS Transistors
     Authors: Yu Lei, Chenchang Zhan, Chenyu Huang and Lidan Wang
     Affiliation: Southern University of Science and Technology, China

205  Title: A Reconfigurable Switched-Capacitor DC-DC Converter and Cascode
     LDO for Dynamic Voltage Scaling and High PSR
     Authors: Yan Lu
     Affiliation: University of Macau, Macao

312  Title: Polyimide-Based Flexible 3-Coil Inductive Link Design and Optimization
     Authors: Yuan Yao, Xiaodong Meng, Chi-Ying Tsui and Wing-Hung Ki
     Affiliation: The Hong Kong University of Science and Technology, Hong Kong
86 Title: A 12-bit 20-MS/s SAR ADC With Fast-Binary-Window DAC Switching in 180nm CMOS
Authors: Yung-Hui Chung, Yi-Shen Lin and Qi-Feng Zeng
Affiliation: National Taiwan University of Science and Technology, Taiwan

97 Title: A 7.8 fJ/conversion-step 9-bit 400-MS/s single-channel SAR ADC with fast control logic
Authors: Zhekan Ni, Yongzhen Chen, Fan Ye and Junyan Ren
Affiliation: Fudan University, Shanghai, China

105 Title: A Transient-Enhanced Digital Low-Dropout Regulator with Bisection Method Tuning
Authors: Da Li, Libo Qian, Xitao He, Jifei Sang and Yinshui Xia
Affiliation: Ningbo University, China

180 Title: A Bandwidth-Tracking Self-Biased 5-to-2800 MHz Low-Jitter Clock Generator in 55nm CMOS
Authors: Naizao Zhong1, Runxi Zhang1, Chunqi Shi1 and Jinghong Chen2
Affiliation: 1. East China Normal University, China
2. University of Houston, USA

185 Title: A Constant-Power Inductive-Coupling Transmitter Using Auxiliary Driving Technique in 65nm SOTB CMOS for Low-Power Supply-Sensing Biosensing Platform toward Healthcare IoTs
Authors: Yuya Nishio, Atsuki Kobayashi and Kiichi Niitsu
Affiliation: Nagoya University, Japan

305 Title: A 7.4 μW Temperature Detecting Circuit for battery monitoring system
Authors: Yanfei Ma1, Zhen Meng2, Shengming Huang1, Yuemin Ding1 and Quanzhen Duan1
Affiliation: 1. Tianjin University of Technology, China
2. Institute of Microelectronics of the Chinese Academy of Sciences, China
PARALLEL SESSION 6

DCS: Digital Circuits and Systems
Session Chair: Chuan Zhang, Southeast University, China
Time: 16:00-18:00 [Room: Longquan]

32 Title: High-Speed Random Number Generator Design in 22nm FD-SOI Process
Authors: Zahit Evren Kaya and Salih Ergün
Affiliation: TUBITAK-Informatics and Information Security Research Center, Turkey

48 Title: Experimental Cryptanalysis of A Chaos-Based Random Number Generator
Authors: İbrahim Taştan and Salih Ergün
Affiliation: Tübitak, Turkey

189 Title: A GALS Design with Opposite-Phase Local Clock Assignment for Power Supply Noise Reduction
Authors: Van Toan Nguyen, Minh Tung Dam and Jeong-Gun Lee
Affiliation: Hallym University, South Korea

203 Title: A Novel Low Voltage DCVSL Circuit Design based on Wilson Current Mirror
Authors: Weiwei Ge¹, Lijuan Han¹, Yuan Cao¹ and Enyi Yao²
Affiliation: 1. Hohai University, China
2. NTU, Singapore

290 Title: Design and hardware implementation of a STT-MRAM based smart card with multiple security algorithms
Authors: Dongsheng Liu¹, Jiawang Hu¹, Cong Zhang¹, Changxing Li¹ and Hualong Zhao²
Affiliation: 1. Huazhong University of Science and Technology, China
2. The 54th institute of China Electronic Technology Group, China

315 Title: Programmable Memristive Threshold Logic Gate Array
Authors: Alex James¹, Olga Krestinskaya² and Akshay Maan¹
Affiliation: 1. Nazarbayev University, Kazakhstan
2. Griffith University, Australia
Day 2, Saturday, October 27, 2018

PARALLEL SESSION 7

CCS: Communication Circuits and Systems
Session Chair: Zhuo Zou, Fudan University, China
Time: 16:00-18:00 [Room: Kangding]

172 Title: A Low-Complexity Mixed-Radix FFT Rotator Architecture
Authors: Wei-Lun Tsai¹, Sau-Gee Chen¹ and Shen-Jui Huang²
Affiliation: 1. National Chiao Tung University, Taiwan
2. Novatek Microelectronics Corp, Taiwan

192 Title: Relaxed Half-Stochastic Iterative Decoding for Rate Compatible Modulation
Authors: Run Zhe Hu, Fang Lu and Yan Dong
Affiliation: Huazhong University of Science and Technology, China

314 Title: Fast and Low-Complexity Decoding Algorithm and Architecture for Quadruple-Error-Correcting RS codes
Authors: Zengchao Yan, Wenjie Li, Jun Lin and Zhongfeng Wang
Affiliation: Nanjing University, China

320 Title: A Low-Complexity Codebook Design for Large-Scale SCMA
Authors: Chao Yang¹, Shusen Jing¹, Xiao Liang¹, Zaichen Zhang¹, Xiaohu You² and Chuan Zhang¹
Affiliation: 1. Southeast University, China
2. National Mobile communication Research Lab., China

321 Title: Adaptive Damped Jacobi Detector and Architecture for Massive MIMO Uplink
Authors: Yaping Zhang¹, Anlan Yu¹, Zaichen Zhang¹, Xiaohu You² and Chuan Zhang¹
Affiliation: 1. Southeast University, China
2. National Mobile communication Research Lab., China

322 Title: An Adjustable Hybrid SC-BP Polar Decoder
Authors: Xiaofeng Zhou¹, Yifei Shen¹, Zaichen Zhang¹, Xiaohu You² and Chuan Zhang¹
Affiliation: 1. Southeast University, China
2. National Mobile communication Research Lab., China
**NDHSI: Nanoelectronics, Devices and Hybrid System Integration**

**Session Chair:** Shaogang Hu, UESTC, China  
**Time:** 16:00-18:00  
**[Room: WangJiang]**

**94**  
**Title:** A Novel 15T-4MTJ based Non-volatile Ternary Content-Addressable Memory Cell for High-Speed, Low-Power and High-Reliable Search Operation  
**Authors:** Deming Zhang, Chengzhi Wang, Lang Zeng, Jie Chen and Weisheng Zhao  
**Affiliation:** Beihang University, China

**107**  
**Title:** MAMI: Majority and Multi-Input Logic on Memristive Crossbar Array  
**Authors:** Debjyoti Bhattacharjee, Arko Dutt and Anupam Chattopadhyay  
**Affiliation:** Nanyang Technological University, Singapore

**181**  
**Title:** Inductance of Different Profiles of Through Glass Vias based on magnetic flux density  
**Authors:** Yang Liu, Zhangming Zhu, Ruixue Ding, Xiaoxian Liu, Qijun Lu, Xiangkun Yin and Yintang Yang  
**Affiliation:** Shaanxi Key Lab. of Integrated Circuits and Systems School of Microelectronics, Xidian University, China

**298**  
**Title:** FPGA Implementation of A Hybrid Decoder for STT-MRAM  
**Authors:** Xue Liu\(^1\), Kui Cai\(^2\) and Zhen Mei\(^2\)  
**Affiliation:** 1. Northeastern University, China  
2. Singapore University of Technology and Design, Singapore

**299**  
**Title:** A 0.5-nW 29ppm/°C Voltage Reference Circuit  
**Authors:** Haoyu Zhuang, Zhangming Zhu, He Tang and Xizhu Peng  
**Affiliation:** University of Science and Technology of China and Xidian University, China

**313**  
**Title:** A NOVEL DUAL DIRECTION SCR WITH DUMMY GATE STRUCTURE FOR HIGH VOLTAGE ESD PROTECTION  
**Authors:** Xiangliang Jin and Yang Wang  
**Affiliation:** Hunan Normal University, China
PARALLEL SESSION 9

AMSC: Analog and Mixed Signal Circuits
Session Chair: Lishan Lv, UESTC, China
Time: 10:35-12:05 [Room: Kangding]

9  Title: A 8-Bit High Speed Successive Approximation Analog-to-Digital Converter
    Authors: Pengyu Gao Wang, Bo Gao and Zheng Qian
    Affiliation: Sichuan University, China

21 Title: Design of A CML Driver Circuit in 28 nm CMOS Process
    Authors: Xinwei Lv and Chunming Zhang
    Affiliation: Xi'an University of Posts and Telecommunications, China

22 Title: Design of High Speed Dynamic Comparator in 28nm CMOS
    Authors: Yuan Cao and Chunming Zhang
    Affiliation: Xi'an University of Posts and Telecommunications, China

195 Title: Switched Capacitor based Area Efficient Positive and Negative Voltage Multiplier
    Authors: Vikas Rana
    Affiliation: STMicroelectronics Pvt Ltd, India

2001 Title: A simple SPICE model for Negative Capacitance Field-Effect Transistors and its applications
    Authors: Chenglong Huang, Liang Fang and Dongdong Hao
    Affiliation: National University of Defense Technology
Title: Low-Complexity LDPC Decoder for 5G URLLC
Authors: Jian-Cheng Liu, Huan-Chun Wang, Chung-An Shen and Jih-Wei Lee
Affiliation: National Taiwan University of Science and Technology, Taiwan

Title: A 25-GS/s 4-bit Single-core Flash ADC in 28 nm FDSOI CMOS
Authors: Yulang Feng and Jinghong Chen
Affiliation: University of Houston, USA

Title: Performance optimization for the CMOS voltage reference circuit based on NSGA-II
Authors: Huajie Huang¹, Yanhan Zeng¹, Jinrui Liao¹ and Hong-Zhou Tan²
Affiliation: 1. Guangzhou University, China
2. Sun Yat-sen University, China

Title: An Automated System for Checking Lithography Friendliness of Standard Cells
Authors: I-Lun Tseng, Yongfu Li, Valerio Perez, Vikas Tripathi, Zhao Chuan Lee and Jonathan Yoong Seang Ong
Affiliation: GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore

Title: Digital PID Based on Pseudo Three-Type Compensation for DC-DC Converter
Authors: Jiajia Wang, Shaowei Zhen, Yajuan He, Penghao Zeng, Jiawei Chen, Wanli Zhou, Ping Luo and Bo Zhang
Affiliation: University of Science and Technology of China, China
PARALLEL SESSION 11

DCS: Digital Circuits and Systems
Session Chair: Letian Huang, University of Electronic Science and Technology of China, China
Time: 10:35-12:05 [Room: Huanglong]

177 Title: A Stochastic Oscillator Using Multiple Ring Oscillators and OR-Gate for Low Voltage Operation in 65 nm CMOS
Authors: Shunya Murakami, Kenya Hayashi, Shigeki Arata, Ge Xu, Cong Dang Bui, Atsuki Kobayashi and Kiichi Niitsu
Affiliation: Nagoya University, Japan

116 Title: Gradualist and Case Experimental Design for Digital Clock Based on Pocket Laboratory
Authors: Shuqun Wang
Affiliation: Southwest Minzu University, China

300 Title: A Novel Design of a 47GHz Programmable Frequency Divider based on RLTSPC Logic in 65nm CMOS
Authors: Xinlin Geng, Qian Xie and Zheng Wang
Affiliation: University of Science and Technology of China

2019 Title: In-Phase Error Self-Calibration For Silicon Microgyroscopes
Authors: Risheng Liu, Yang Zhao, Guoming Xia, Anping Qiu, Qin Shi and Yazhou Wang
Affiliation: Nanjing University of Science and Technology

294 Title: Design of an Energy-Autonomous Supply-Sensing Biosensor Platform Using Biofuel Cells and Human-Body-Communication Transmitter
Authors: Keisuke Kayano, Maya Matsunaga, Keisuke Itakura, Atsuki Kobayashi and Kiichi Niitsu
Affiliation: Nagoya University, Japan
Parallel Session 12

ICS: IoT Circuits and Systems
Session Chair: Guoxing Wang, Shanghai Jiao Tong University, China
Time: 10:35-12:05 [Room: Longquan]

2010 Affiliation: Design and Implementation of Portable Sensory System for Air Pollution Monitoring
Authors: Xuan Zhao, Rami Ghannam, Qammer H Abbasi and Hadi Heidari
Affiliation: University of Glasgow

2011 Affiliation: Smart Multi-Sensory Ball for Water Quality Monitoring
Authors: Yusu Wang, Rami Ghannam and Hadi Heidari
Affiliation: University of Glasgow

2013 Affiliation: A compact Non-Invasive Wearable Vital Signal Monitoring System
Authors: Yuan Wei, Adnan Zahid, Hadi Heidari, Muhammad Imran and Qammer H. Abbasi and Siming Zuo
Affiliation: University of Glasgow

2014 Affiliation: A Compact Wearable System for Detection and Estimation of Open Wound Status in Diabetic Patients
Authors: Zhengnan Yuan, Jiaxing Huang, Zhiqin Zhao, Adnan Zahid, Hadi Heidari, Rami Ghannam and Qammer H. Abbasi and Siming Zuo
Affiliation: Hong Kong University of Science and Technology

2015 Affiliation: A Compact Wearable System for Detection of Plantar Pressure for Diabetic Foot Prevention
Authors: Zihang You, Adnan Zahid, Hadi Heidari, Muhammad Ali Imran and Qammer H. Abbasi
Affiliation: Glasgow College, University of Electronics Science and Technology of China
PARALLEL SESSION 13

DSP: Digital Signal Processing
Session Chair: Shuyan Jiang, University of Science and Technology of China & Xiaoping Zeng, Chongqing University, China
Time: 14:00-16:00 [Room: Kangding]

7 Title: A Branch-and-Bound Algorithm with Reduced Search Space for Sparse Filter Design
   Authors: Wangqian Chen¹, Xin Lou² and Mo Huang¹
   Affiliation: 1. South China University of Technology, Guangzhou, China
               2. Shanghai Tech University, Shanghai, China

100 Title: Analysis on the Two Dimensional Spectrum of Squint-Looking SAR with Constant Acceleration
   Authors: Hui Xu¹, Yingqin Sun² and Yong Wang²
   Affiliation: 1. Xi’an Research Institute of Applied Optics, China
               2. Suzhou Toursight Electronics Co. Ltd., China

266 Title: Reform and Practice of Analog Circuits
   Authors: Hua Fan
   Affiliation: University of Science and Technology of China, China

267 Title: How to Construct a Resonable Teaching Quality Assurance System in Universities
   Authors: Jin Zhang, Hua Fan, Man Fang and Weijian Chen
   Affiliation: University of Science and Technology of China, China

334 Title: Utilization of Process and Supply Voltage Random Variations for Random Bit Generation
   Authors: Moshe Avital, Anatoli Mordakhay, David Zooker Zabib, Yoav Weizman, Alexander Fish and Osnat Keren
   Affiliation: Bar-Ilan University, Israel
Day 3, Sunday, October 28, 2018

PARALLEL SESSION 14

AMSCS: Analog and Mixed-Signal Circuits and Systems
Session Chair: Zhang Zhang, HFUT, China
Time: 14:00-16:00 [Room: WangJiang]

11  Title: Sub-Volt Bulk-Driven Transconductance Amplifier and Filter Application
    Authors: Montree Kumngern
    Affiliation: King Mongkut’s Institute of Technology Ladkrabang, Thailand

183 Title: A 10-bit 0.64 to 1.27-mW 20-MS/s Hybrid Digital-to-Analog Converter with a Power Control Logic
    Authors: Qinjin Huang¹ and Fengqi Yu²
    Affiliation: 1. School of Electronic and Communication Engineering, Shenzhen Polytechnic, China
              2. Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, China

187 Title: A BER-Modulated 3-Coil Inductive-Coupling Transceiver Using Dynamic Intermediate Interference Control Technique
    Authors: Ge Xu, Kenya Hayashi, Shigeki Arata, Shunya Murakami, Cong Dang Bui, Atsuki Kobayashi and Kiichi Niitsu
    Affiliation: Nagoya University, Japan

199 Title: Switched Capacitor based High Positive and Negative Voltage Charge-pump using Sample and Hold technique
    Authors: Vikas Rana and Abhishek Mittal
    Affiliation: STMicroelectronics Pvt. Ltd., India

304 Title: Review of Solar Energy Harvesting for IoT Applications
    Authors: Ping Luo, Dingming Peng, Yuanfei Wang and Xinyi Zheng
    Affiliation: University of Science and Technology of China, China

333 Title: A 0.65-V 10-bit 320kS/s SAR-ADC with Charge Average and Skip Switching Algorithm
    Authors: Yi-Han Ou-Yang, Cheng-Chun Wu and Kea-Tiong Tang
    Affiliation: National Tsing Hua University, Taiwan
**Day 3, Sunday, October 28, 2018**

**PARALLEL SESSION 15**

**DA: Design Automations**  
Session Chair: Yongfu Li, GLOBALFOUNDRIES  
Time: 14:00-16:00  
[Room: Huanglong]

<table>
<thead>
<tr>
<th>#</th>
<th>Title</th>
<th>Authors</th>
<th>Affiliation</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Title: An efficient variable-gain homotopy method for finding DC operating points of transistor circuits</td>
<td>Authors: Kiyotaka Yamamura and Takumi Shimada</td>
<td>Affiliation: Chuo University, Japan</td>
</tr>
<tr>
<td>19</td>
<td>Title: Finding all solutions of piecewise-linear resistive circuits using triangular LP test</td>
<td>Authors: Kiyotaka Yamamura and Hiroki Takahara</td>
<td>Affiliation: Chuo University, Japan</td>
</tr>
<tr>
<td>49</td>
<td>Title: Decimal Multiplication Using Combination of Software and Hardware</td>
<td>Authors: Riaz-Ulhique Mian, Michihiro Shintani and Michiko Inoue</td>
<td>Affiliation: NAIST, Japan</td>
</tr>
<tr>
<td>117</td>
<td>Title: Symbolic Circuit Reduction for Multistage Amplifier Macromodeling</td>
<td>Authors: Hao Yu and Guoyong Shi</td>
<td>Affiliation: Shanghai Jiao Tong University, China</td>
</tr>
<tr>
<td>170</td>
<td>Title: A Novel Compiler for Regular Expression Matching Engine Construction</td>
<td>Authors: Xin Jin, Lin Jun and Zhongfeng Wang</td>
<td>Affiliation: Nanjing University, China</td>
</tr>
<tr>
<td>200</td>
<td>Title: Analytical Modeling of Process Variability in Subthreshold Regime for Ultra Low Power Applications</td>
<td>Authors: Anala M and B P Harish</td>
<td>Affiliation: University Visvesvaraya College of Engineering, Bangalore, India</td>
</tr>
</tbody>
</table>
Title: A Nanopower 4th-order Chebyshev Lowpass Filter For ECG Detection System  
Authors: Prajub Pawarangkoon  
Affiliation: Mahanakorn University of Technology, Thailand

Title: Heart Rate Estimation from Ballistocardiography Based on Hilbert Transform and Phase Vocoder  
Authors: Qingsong Xie, Guoxing Wang and Yong Lian  
Affiliation: Shanghai Jiao Tong University, Shanghai, China

Title: A Fully Integrated Chopper IA for Implantable Multichannel EEG Recording Without Impedance Boosting Circuits  
Authors: Liang Zhiming, Li Bin and Wu Zhaohui  
Affiliation: South China University of Technology, China

Title: An Overview of the Recent Digital Low Drop-out Regulator Design Trend  
Authors: Mo Huang¹ and Yan Lu²  
Affiliation: 1. South China University of Technology, China  
2. State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao

Title: A Heart Rate Measurement System Based on Ballistocardiogram for Smart Furniture  
Authors: Ziran He¹, Yong Lian², Guoxing Wang¹, Zhengchun Peng³, Yang Zhao², Min Wang¹ and Bo Meng³  
Affiliation: 1. Shanghai Jiao Tong University, China,  
2. University of York, Canada  
3. Shenzhen University, China

Title: A High Accuracy and High Sensitivity System Architecture for Electrical Impedance Tomography System  
Authors: Hui Li, Boxiao Liu, Yongfu Li, Guoxing Wang and Yong Lian  
Affiliation: Shanghai Jiao Tong University, China
Day 4, Monday, October 29, 2018

PARALLEL SESSION 17

NNNE: Neural Networks and Neuromorphic Engineering
Session Chair: Letian Huang, University of Electronic Science and Technology of China, China
Time: 08:40-10:10 [Room: Kangding]

Title: Patterns Detection and Recognition in Visual Aided System for Prosthesis Pose Estimation during Total Hip Replacement Surgery
Authors: Syed Mudassir, Shaojie Su, Mingzhu Long and Zhihua Wang
Affiliation: Tsinghua University, China

Title: Frontalization with Adaptive Exponentially-Weighted Average Ensemble Rule for Deep Learning Based Facial Expression Recognition
Authors: Kai-Yuan Tsai, Jian-Jiun Ding and Yih-Cherng Lee
Affiliation: National Taiwan University, Taiwan

Title: Dolphin Recognition with Adaptive Hybrid Saliency detection for Deep Learning Based on DenseNet Recognition
Authors: Hung-Wei Hsu¹, Yih-Cherng Lee¹, Jian-Jiun Ding¹ and Ronald Y. Chang²
Affiliation: 1. National Taiwan University, Taiwan
2. Research Center for Information Technology Innovation, Academia Sinica, Taiwan

Title: A Circuit Implementation Method for Memristor Crossbar with On-chip Training
Authors: Yonglei Zhao and Guoyong Shi
Affiliation: Shanghai Jiao Tong Univ., China

Title: LSTM network hardware architecture for time-series predictive modeling problems
Authors: Alex James, Kamilya Smagulova and Kazybek Adam
Affiliation: Nazarbayev University, Kazakhstan
Title: Image Denoising Algorithms for DoFP Polarization Image Sensors with Non-Gaussian Noises  
Authors: Shiting Li, Wenbin Ye, Xiaofang Pan and Xiaojin Zhao  
Affiliation: Shenzhen University, China

Title: Accurate Road Detection from Satellite Images Using Modified U-net  
Authors: Alexandre Constantin, Jian-Jiun Ding and Yih-Cherng Lee  
Affiliation: National Taiwan University, Taiwan

Title: CMOS Image Sensor Data-Readout Method for Convolutional Operations with Processing Near Sensor Architecture  
Authors: Huifeng Zhu, Qi Wei, Fei Qiao, Yi Yang, Xinjun Liu, Shuzheng Xu and Huazhong Yang  
Affiliation: Tsinghua University, China

Title: Transistor Sizing for Parameter Obfuscation of Analog Circuits Using Satisfiability Modulo Theory  
Authors: Vaibhav Venugopal Rao and Ioannis Savidis  
Affiliation: Drexel University, United States

Title: Down Conversion Mixer with Low/High Band Re-configurable Transconductance Amplifier in 65nm CMOS Process  
Authors: Nisha Gupta, Ashudeb Dutta and Shiv Govind Singh  
Affiliation: IIT Hyderabad, India
93 Title: Multi-Scale Multi-Domain Co-Simulation for Rapid ADAS Prototyping  
Authors: Róbert Lajos Bücs, Rainer Leupers and Gerd Ascheid  
Affiliation: RWTH Aachen University, Germany

288 Title: Low-cost vector map assisted navigation strategy for autonomous vehicle  
Authors: Wenda Li¹, Xianjie Meng¹, Zheng Wang², Wenqi Fang², Jie Zou² and Huiyun Li²  
Affiliation: 1. Shandong University of Technology, China  
2. Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, China

289 Title: A CGRA Based AI Inference Engine Supporting Supervised and Reinforcement Learning  
Authors: Minglan Liang¹, Mingsong Chen¹ and Zheng Wang²  
Affiliation: 1. Guilin University of Electronic Technology, China  
2. Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, China

291 Title: Accelerator design for convolutional neural network with vertical data streaming  
Authors: Shanliao Li¹, Ning Ouyang¹ and Zheng Wang²  
Affiliation: 1. Guilin University of Electronic Technology, China  
2. Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, China

295 Title: Secure and Tamper-resilient Distributed Ledger for Data Aggregation in Autonomous Vehicles  
Authors: Sananda Mitra¹, Sumanta Bose², Sourav Sen Gupta² and Anupam Chattopadhyay²  
Affiliation: 1. Techno India College of Technology, India  
2. Nanyang Technological University, Singapore
Title: On Comparing AES and ChaCha20 in Side-Channel Context
Authors: Zakaria Najm¹, Dirmanto Jap¹, Bernhard Jungk¹, Stjepan Picek² and Shivam Bhasin³
Affiliation: 1. Nanyang Technological University, Singapore
2. Delft University of Technology, Netherlands
3. Temasek Labs@NTU, Singapore
Title: A Comparative Study of Modeling Attacks On Arbiter PUF
Authors: Yue Fang¹, Qingqing Ma¹, Chongyan Gu², Chenghua Wang¹, Maire O’Neill² and Weiqiang Liu¹
Affiliation: 1. Nanjing University of Aeronautics and Astronautics, China
2. Queen’s University Belfast, UK

Title: Lightweight Hardware Implementation of R-LWE Lattice-Based Cryptography
Authors: Sailong Fan¹, Weiqiang Liu¹, James Howe², Ayesha Khalid³ and Maire O’Neill³
Affiliation: 1. Nanjing University of Aeronautics and Astronautics, China
2. University of Bristol, UK
3. Queen’s University Belfast, UK

Title: Error Samplers for Lattice-Based Cryptography - Challenges, Vulnerabilities and Solutions
Authors: Ayesha Khalid¹, Ciara Rafferty¹, James Howe², Séamus Brannigan¹, Weiqiang Liu³ and Máire O’Neill¹
Affiliation: 1. Centre for Secure Information Technologies (CSIT), ECIT, Queen’s University Belfast, UK
2. University of Bristol, UK
3. Nanjing University of Aeronautics and Astronautics, China

Title: A Deep Learning Modeling Attack Method for MISR-APUF Protection Structures
Authors: Ge Wei¹, Huang Jiquan¹, Liu Bo¹, Zhu Min² and Cao Yuan³
Affiliation: 1. Southeast University, China
2. Kate Microelectronics corporation, China
3. Hohai University, China
Title: Lazy Reduction and Multi-Precision Division Based on Modular Reductions
Authors: Shuguo Li and Zhen Gu
Affiliation: Tsinghua University, China

Title: Security Path Verification Through Joint Information Flow Analysis
Authors: Wei Hu, Xinmu Wang and Dejun Mu
Affiliation: Northwestern Polytechnical University, China
PARALLEL SESSION 21

SSE 1: Emerging Threats in the IoT Era: Chip Reliability and Security
Session Chair: Xiaohang Wang, South China University of Technology, China
Time: 10:30-12:00 [Room: Kangding]

114 Title: CoLPUF: A Novel Configurable LFSR-based PUF
Authors: Srinivasu Bodapati, Vikramkumar Pudi, Anupam Chattopadhyay and Kwok Yan Lam
Affiliation: Nanyang Technological University, Singapore

115 Title: Capacitance Measurement of Running Hardware Devices and its Application to Malicious Modification Detection
Authors: Makoto Nishizawa, Kento Hasegawa and Nozomu Togawa
Affiliation: Waseda University, Japan

208 Title: Importance of Multi-parameter SAT Attack Exploration for Integrated Circuit Security
Authors: Kyle Juretus and Ioannis Savidis
Affiliation: Drexel University, United States

307 Title: Enhancing Physical Unclonable Function Robustness Employing Embedded Instruments
Authors: Jerrin Pathrose, Ghazanfar Ali and Hans Kerkhoff
Affiliation: University of Twente, Netherlands

318 Title: A New Error Correction Scheme for Physical Unclonable Function
Authors: Sun Kai¹, Yifei Shen¹, Yingjie Lao², Zaichen Zhang¹, Xiaohu You¹ and Chuan Zhang¹
Affiliation: 1. Southeast university, China
2. Clemson University, United States
95 Title: Novel Adaptive Rood Path Searches with Small Motion Prejudgments for Fast Block Motion Estimation
Authors: Hung-Yi Chen, Jian-Jiun Ding and Yih-Chereng Lee
Affiliation: National Taiwan University, Taiwan

273 Title: Benchmark of RRAM based Architectures for Dot-Product Computation
Authors: Xiaochen Peng¹ and Shimeng Yu²
Affiliation: 1. Arizona State University, United States
2. Georgia Institute of Technology, United States

282 Title: High-Density and Fast-Configuration Non-Volatile Look-Up Table Based on NAND-Like Spintronic Memory
Authors: He Zhang, Wang Kang, Zhaohao Wang, Youguang Zhang and Weisheng Zhao
Affiliation: Beihang University, China

283 Title: Stability and Variability Emphasized STT-MRAM Sensing Circuit With Performance Enhancement
Authors: Menglin Han¹, Hao Cai¹, Jun Yang¹, Lirida Naviner², You Wang³ and Weisheng Zhao³
Affiliation: 1. Southeast University, China
2. Télécom-ParisTech, Université Paris-Saclay, France
3. Beihang University, China

326 Title: ReRAM-based Circuit and System Design for Future Storage and Computing
Authors: Chenchen Liu and Tong Wu
Affiliation: Clarkson University, United States

337 Title: A Probabilistic Prediction Based Fixed-Width Booth Multiplier
Authors: Yajuan He
Affiliation: University of Science and Technology of China, China
PARALLEL SESSION 23

**SSE7: Design and Implementation for Advanced Baseband Signal Processing**

**Session Chair:** Shan Cao, Shanghai University, China

**Time:** 10:30-12:00  
**[Room: Huanglong]**

**297**  
**Title:** A Unified Reconfigurable Datapath for 5G Compatible LDPC Decoding  
**Authors:** Ting Lin, Shan Cao, Shunqing Zhang and Shugong Xu  
**Affiliation:** Shanghai University, China

**319**  
**Title:** LDPC Decoder Based on Markov Chain Monte Carlo Method  
**Authors:** Jiejun Jin, Xiao Liang, Zaichen Zhang, Xiaohu You and Chuan Zhang  
**Affiliation:** Southeast University, China

**330**  
**Title:** A High-Speed and Low-Complexity Architecture for Softmax Function in Deep Learning  
**Authors:** Meiqi Wang, Siyuan Lu, Danyang Zhu, Jun Lin and Zhongfeng Wang  
**Affiliation:** School of Electronic Science and Engineering, Nanjing University, China

**331**  
**Title:** Analysis of the Dual-Threshold-Based Shrinking Scheme for Effective NB-LDPC Decoding  
**Authors:** Jing Tian, Jun Lin and Zhongfeng Wang  
**Affiliation:** Nanjing University, China

**332**  
**Title:** Low Cost LSTM Implementation based on Stochastic Computing for Channel State Information Prediction  
**Authors:** Shuai Li, Xiaojie Liu and Jienan Chen  
**Affiliation:** University of Science and Technology of China
PARALLEL SESSION 24

SSE5: Artificial Intelligent (AI) System and Advanced Processing (AP) Core Technology
Session Chair: Hongbin Sun, Xi'an Jiaotong University, China
Time: 10:30-12:00 [Room: Longquan]

269 Title: Calibration of Low-Cost Particle Sensors by Using Machine-Learning Method
Authors: Chen-Chia Chen, Chih-Ting Kuo, Ssu-Ying Chen, Chih-Hsing Lin, Jin-Ju Chue, Yi-Jie Hsieh, Chun-Wen Cheng, Chieh-Ming Wu and Chun-Ming Huang
Affiliation: National Chip Implementation Center, Taiwan

280 Title: Type-4 2-D Diagonal and Four-Fold Rotational Symmetry Digital Filter Architectures
Authors: Lan-Da Van¹, Tsung-Che Lu¹, Pei-Yu Chen¹ and Hari C. Reddy²
Affiliation: 1. National Chiao Tung University, Taiwan
2. California State University, Long Beach, United States

296 Title: Intelligent Vehicle Collision-Avoidance System with Deep Learning
Authors: Yeong-Kang Lai, Yu-Hau Huang, Chuan-Wei Huang, Yi-Xian Kuo and Yu-Chieh Chung
Affiliation: National Chung Hsing University, Taiwan

306 Title: Acceleration of Depth Intra Coding for 3D-HEVC by Efficient Early Termination Algorithm
Authors: Yu-Chih Hsu¹, Jie-Ru Lin¹, Mei-Juan Chen¹, Chia-Hung Yeh² and Min-Hui Lin³
Affiliation: 1. National Dong Hwa University, Taiwan
2. National Taiwan Normal University, Taiwan
3. National Sun Yat-sen University, Taiwan

284 Title: A 4K×2K@60fps Multi-format Multi-function Display Processor for High Perceptual Quality
Authors: Hang Wang¹, Hongbin Sun¹, Xuchong Zhang¹, Qiubo Chen¹, Pengju Ren¹, Xiaogang Wu¹, Shouyi Yin², Zhiqiang Jiang³, Xiang Li³, Daqiang Han³, Shiquan Yu³, Shaojun Wei² and Nanning Zheng¹
Affiliation: 1. Xi'an Jiaotong University, China
2. Tsinghua University, China
3. Changhong Electric, China
Title: Study of High Voltage Deep Brain Stimulation
Authors: Zhang Zhang, Lingling Wei, Xiaojuan Zhou, Taolue Zhu, Guangjun Xie and Xin Cheng
Affiliation: HFUT, China
**Poster Sessions**

**POSTER SESSION 1**

**Session Chair: Zhuo Zou, Fudan University**

**Time: 15:30-16:00, October 27, 2018**

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<td>Tian Qiaoyu, Wang Yinan, Liu Guiqing, Liu Xiangyu, Diao Jietao and Xu Hui</td>
<td>National University of Defense Technology, China</td>
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<td>196 High-Efficiency Wilkinson-Power-Combining Class-EF Amplifier with Lumped-Element Load Network</td>
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<td>212 A Supply Noise Compensation Circuit for Clock Buffers to Reduce Timing Jitter</td>
<td>Jing Li, Jian Luo, Yongfeng Ding and Ning Ning</td>
<td>University of Science and Technology of China, China</td>
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<td>279 Teaching Practice Platform and Innovation Course Construction for Postgraduate Majoring in Electronics Information</td>
<td>Kuojun Yang¹, Peng Ye¹, Duyu Qiu¹ and Jiali Shi²</td>
<td>1. University of Science and Technology of China, China 2. SiChuan College of Architectural Technology, China</td>
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<td>292 The Design and Miniaturization of 6-15 GHz Lumped-Element Wilkinson Power Divider Based on GaAs IPD Technology</td>
<td>Yang Chen, Xu Yan, Han Wu and Liguo Sun</td>
<td>University of Science and Technology of China, China</td>
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<td>311 A 40.68MHz Active Rectifier with Hybrid Delay Compensation Scheme</td>
<td>Langyu Hu, Lin Cheng, Yuan Yao, Tak Sang Yim, Wing-Hung Ki and Chi Ying Tsui</td>
<td>The Hong Kong University of Science and Technology, Hong Kong,</td>
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Session Chair: Xiong Zhou, UESTC, China  
Time: 10:05-10:35, October 28, 2018

13  Title: An Area-Efficient Differential Serial DAC with Mismatch Compensation Scheme  
Authors: Chen-I Chiu and Kea-Tiong Tang  
Affiliation: National Tsing Hua University, Hsinchu, Taiwan

14  Title: A Radiation-Hardened Trench Power MOSFET for Aerospace Applications  
Authors: Feng Yang, Hao Wu, Xiaojun Fu, Fan Xiang, Zhi Zheng and Fei Xiang  
Affiliation: Sichuan Institute of Solid-State Circuits, China

33  Title: A Fast-Response BUCK Converter with Adaptive Detect and Transient Enhancement Techniques  
Authors: Zekun Zhou\textsuperscript{1}, Junyuan Rong\textsuperscript{1}, Yue Shi\textsuperscript{2} and Bo Zhang\textsuperscript{1}  
Affiliation: 1. University of Science and Technology of China, China  
2. Chengdu University of Information Technology, China

35  Title: A Time-domain Bandgap Reference with Continuous Output Voltage  
Authors: Zekun Zhou\textsuperscript{1}, Hongming Yu\textsuperscript{1} and Yue Shi\textsuperscript{2}  
Affiliation: 1. University of Science and Technology of China, China  
2. Chengdu University of Information Technology, China

36  Title: A Bandgap Reference Using a Novel self-start Bias Circuit  
Authors: Zekun Zhou\textsuperscript{1}, Yunkun Wang\textsuperscript{1} and Yue Shi\textsuperscript{2}  
Affiliation: 1. University of Science and Technology of China, China  
2. Chengdu University of Information Technology, China

38  Title: Study of Music Effect on Mental Stress Relief Based on Heart Rate Variability  
Authors: Maya Chennafi, Muhammad Adeel Khan, Gang Li, Lian Yong and Wang Guoxing  
Affiliation: Shanghai Jiao Tong University, China

89  Title: A Novel Digitally-Controlled DC Offset Calibration Circuit for the Chopper Instrumentation Amplifier  
Authors: Yi Zhang, Lianxi Liu and Tianyuan Hua  
Affiliation: School of Microelectronics in Xidian University, China

99  Title: A 10-KS/s 625-Hz-Bandwidth 60-dB SNDR Noise-Shaping ADC for Bio-potential Signals Detection Application
Authors: Jin Hu, Maliang Liu, Shubin Liu, Ruixue Ding and Zhangmin Zhu
Affiliation: Xidian University, China
Session Chair: Yongming Li, Chongqing University
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102 Title: A Simplified PWM Controller for Wireless Power Receiver Using a 3-Mode Reconfigurable Resonant Regulating Rectifier
Authors: Lin Cheng, Xinyuan Ge, Wing-Hung Ki and Chi-Ying Tsui
Affiliation: The Hong Kong University of Science and Technology, Hong Kong

106 Title: Area-Efficient Scheduling Scheme Based FFT Processor for Various OFDM Systems
Authors: Jeong Keun Jang¹, Ho Keun Kim², Myung Hoon Sunwoo² and Oscar gustafsson³
Affiliation: 1. Dongbu Hitek, South Korea
2. Ajou University, South Korea
3. Oscar Gustafsson, Linkoping University, Sweden

110 Title: A Background Timing Skew Calibration Technique in Time-Interleaved ADCs With Second Order Compensation
Authors: Dengquan Li, Ruixue Ding, Zhangming Zhu and Yintang Yang
Affiliation: Xidian University, China

112 Title: FPGA implementation of edge detection for Sobel operator in eight directions
Authors: Zou Xiangxi, Zhang Yonghui, Zhang Shuaiyan and Zhang Jian
Affiliation: Hainan University, China

169 Title: Forward Modeling Assisted Digital Predistortion Method for Hybrid Beamforming Transmitters with a Single PA Feedback
Authors: Hongmin Li, Gang Li, Yikang Zhang, Wen Qiao and Falin Liu
Affiliation: University of Science and Technology of China, China

174 Title: A CMOS Temperature Sensor With Single-Point Calibration for Retinal Prosthesis
Authors: Zhiheng Zheng, Mingyi Chen, Jie Zhou and Guoxing Wang
Affiliation: Shanghai Jiao Tong University, China

175 Title: A 100 μW AC-DC Boost Converter for Electromagnetic Energy Harvesting With 0.2 VPeak Self-starting Voltage and 85% Efficiency
Authors: Kangqi Liu¹, Mingyi Chen¹, Yiyu Gong², Songhai Fan² and Guoxing Wang¹
Affiliation: 1. Shanghai Jiao Tong University, China  
2. Electric power research institute of State Grid Sichuan Corporation of China

310 A Voltage Swing Robust Pseudo-Resistor Structure for Biomedical Front-end Amplifier  
Sanfeng Zhang, Xiong Zhou and Qiang Li  
University of Science and Technology of China, China
Brief Introduction of Electronic Science and Technology Museum in UESTC

Electronic Science and Technology Museum is the first comprehensive museum about electronic science and technology in China, which aims at recording important characters and events that promoted the development of electronic science and technology, especially in China, by using representative devices in the history of the development of electronic science and technology. It was proposed in April, 2015 and established in September, 2016.

Next to the lake which is in the west of campus and located the Academic lecture hall 1F, the Museum covers an area of about 2,000 square meters in the Qingshuihe Campus of UESTC. It consists of 6 units, including communication, radar, radio & television, electronic measuring instruments, electronic components and computers.

Adopting the method of displaying, museum combines online and offline with indoor and outdoor, which fully plays a role in Professional education, scientific research, cultural inheritance, and serving teachers and students in schools, alumni, profession and the whole society.

<table>
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<tr>
<th>中文名称</th>
<th>English</th>
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<tr>
<td>第一单元: 通信展厅</td>
<td>Part I: Communication Hall</td>
</tr>
<tr>
<td>1.电报</td>
<td>Telegraphy</td>
</tr>
<tr>
<td>2.电话与交换设备</td>
<td>Telephone and switch equipment</td>
</tr>
<tr>
<td>3.无线与移动通信</td>
<td>Wireless and mobile communication</td>
</tr>
<tr>
<td>中文名称</td>
<td>English</td>
</tr>
<tr>
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<td>----------</td>
</tr>
<tr>
<td>第二单元：雷达展厅</td>
<td>Part II: Radars Hall</td>
</tr>
<tr>
<td>军用雷达</td>
<td>Military radar</td>
</tr>
<tr>
<td>民用雷达</td>
<td>Civil radar</td>
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<tr>
<th>中文名称</th>
<th>English</th>
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<td>第三单元：广播电视展厅</td>
<td>Part III: Radios and Televisions Hall</td>
</tr>
<tr>
<td>广播</td>
<td>Radio</td>
</tr>
<tr>
<td>电视</td>
<td>Television</td>
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<tr>
<th>中文名称</th>
<th>English</th>
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<tr>
<td>第四单元：电子测量仪器展厅</td>
<td>Part IV: Electronic Measuring Instruments Hall</td>
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<tr>
<td>模拟时代</td>
<td>Analog machine era</td>
</tr>
<tr>
<td>数字时代</td>
<td>Digital machine era</td>
</tr>
<tr>
<td>智能时代</td>
<td>Intelligent machine era</td>
</tr>
<tr>
<td>虚拟时代</td>
<td>Virtual machine era</td>
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<th>中文名称</th>
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<td>第五单元：电子元器件展厅</td>
<td>Part V: Electronic Components Hall</td>
</tr>
<tr>
<td>第六单元：计算机单元</td>
<td>Computers Hall</td>
</tr>
<tr>
<td>展望未来</td>
<td>Future Prospect</td>
</tr>
<tr>
<td>序厅</td>
<td>Preface Hall</td>
</tr>
<tr>
<td>Exhibits</td>
<td>Description of Exhibits</td>
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<tr>
<td>----------</td>
<td>-------------------------</td>
</tr>
<tr>
<td><strong>通信单元</strong> (Communication)</td>
<td></td>
</tr>
<tr>
<td>西藏 450MHz 通信系统 “好易通”基站</td>
<td>450MHz &quot;Haoyitong&quot; Communication Base Station</td>
</tr>
<tr>
<td>华为 C&amp;C08 数字程控交换机</td>
<td>Huawei C&amp;C08 Digital and Program-Controlled Switch</td>
</tr>
<tr>
<td>BD055 型电传打字机</td>
<td>BD055 Teletypewriter</td>
</tr>
<tr>
<td>马可尼收讯机和发射机</td>
<td>Marconi Receivers and Transmitters</td>
</tr>
<tr>
<td><strong>雷达单元</strong> (Radar)</td>
<td></td>
</tr>
<tr>
<td>X 波段大天线阵列成像雷达实验系统</td>
<td>X-Band Imaging Radar Experimental System</td>
</tr>
<tr>
<td>大功率速调管</td>
<td>High-Power Klystron</td>
</tr>
<tr>
<td>860 炮瞄雷达</td>
<td>860 Gun-Pointing Radar Vehicle</td>
</tr>
<tr>
<td><strong>广播电视单元</strong> (Radio &amp; Television)</td>
<td></td>
</tr>
<tr>
<td>北京牌 825-2 型电子管黑白电视机</td>
<td>Beijing-Brand 825-2 Vacuum Tube Monochrome Television</td>
</tr>
<tr>
<td>钢丝录音机</td>
<td>Wire Recorder</td>
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### Electronic Components

<table>
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<tr>
<th>Item</th>
<th>Description</th>
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<tr>
<td>Hiview</td>
<td>The first digital video processing chip with proprietary intellectual property rights of China</td>
</tr>
<tr>
<td>Terahertz Gyrotron</td>
<td>Chinese first 220GHz terahertz gyrotron developed independently by UESTC.</td>
</tr>
<tr>
<td>Negative-Resistance Magnetron</td>
<td>The component produced in the United State in 1930s~1940s.</td>
</tr>
</tbody>
</table>
### 波导元件
- **Waveguide Component**
- **It was produced by UESTC according to the Soviet Union’s expert Lebedev’s drawings in 1958.**

### 计算机
- **Computer**

<table>
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<th>计算机名</th>
<th>英文名</th>
<th>描述</th>
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<tr>
<td>DJS 131 小型数字计算机</td>
<td>DJS 131 Small-Sized Digital Computer</td>
<td>The small-sized digital computer was produced by Chinese independently in 1970s.</td>
</tr>
<tr>
<td>龙芯</td>
<td>Chips of Godson Series</td>
<td>The first general-purposed CPU exploited independently by China</td>
</tr>
<tr>
<td>银河壹号巨型计算机</td>
<td>Galaxy-I Super Computer</td>
<td>The first super computer in China with the operation speed exceeding 100 million times per second was produced by Computer Research Institute in National University of Defense and Technology in Changsha city in 1983.</td>
</tr>
<tr>
<td>Apple-II 个人电脑</td>
<td>Apple-II PC</td>
<td></td>
</tr>
</tbody>
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![Image 1](image1.png)

![Image 2](image2.png)
One Day Tour

(Gather at Lobby of Shangri-La Hotel at 8:15 and Set out at 8:30)

Chengdu Research Base for Giant Panda Breeding (成都大熊猫繁育研究基地)
Located just 6 miles (10km) from downtown Chengdu, this is the most convenient place for visitors to see the giant pandas at a close range.
It opened to the public in 1988 and now consists of a research center, an open research laboratory, a veterinary hospital, an enclosure, and a playground for giant pandas. It is regarded as the most important panda sanctuary in the world dedicated to the protection of the giant pandas and other endangered species.

Kuan & Zhai Alley (宽窄巷子)
Being in the list of Chengdu Historical and Cultural Protection Project, Kuan & Zhai Alley historical & cultural district consists of Kuan Lane, Zhai Lane and Jing Lane, which are in parallel arrays running from east to west with a group of quadrangles. It is one of the three major historical & cultural conservation areas in Chengdu, it is not only the last relic of the city pattern of "thousand-year-old young city" and the one-hundred-year original architectural structure of old Chengdu, but also the only existing copy in southern China from the lane (Hutong) culture and architectural style of northern China. According to the plan, the control area is 479mu (1mu=1/15 hectare), in which the kernel conservation area covers 108mu.

Wuhou Shrine Museum (武侯祠)
Located in the south of Chengdu's city center, the Wuhou Shrine (Temple of Marquis Wu) is the most influential museum of the Three Kingdoms (220AD - 280AD) culture in China. Integrated with tombs of Liu Bei (161AD - 223AD), the king of Shu, and Zhuge Liang (181AD - 234AD), a great military and political strategist and Prime Minister of the Shu, the shrine was built in the Western Jin Period (265AD - 316AD).

Jinli Ancient Street (锦里)
Right next to the Wuhou Shrine is Jinli Promenade, a rebuilt trading and folk art street imitating the ancient-style buildings in West Sichuan. "Jinli" is the name of an old street in Han-dynasty Chengdu, meaning "make perfection still more perfect and hide the universe in the universe". The ancient Jinli was one of the oldest and the most commercialized streets in the history of West Shu and had been well-known throughout the country in Qin, Han, and Three Kingdoms Periods.
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